FIG. 1

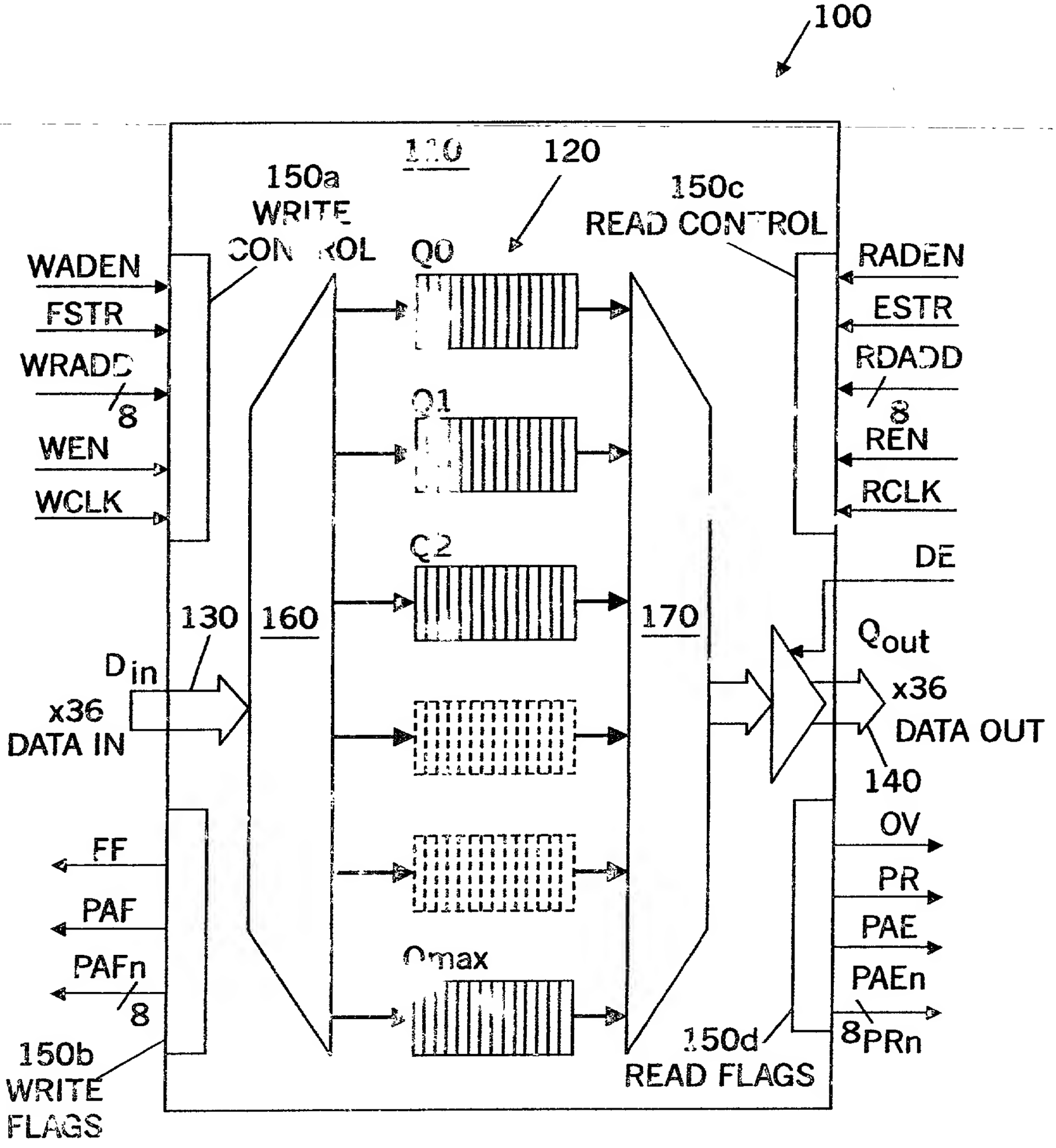
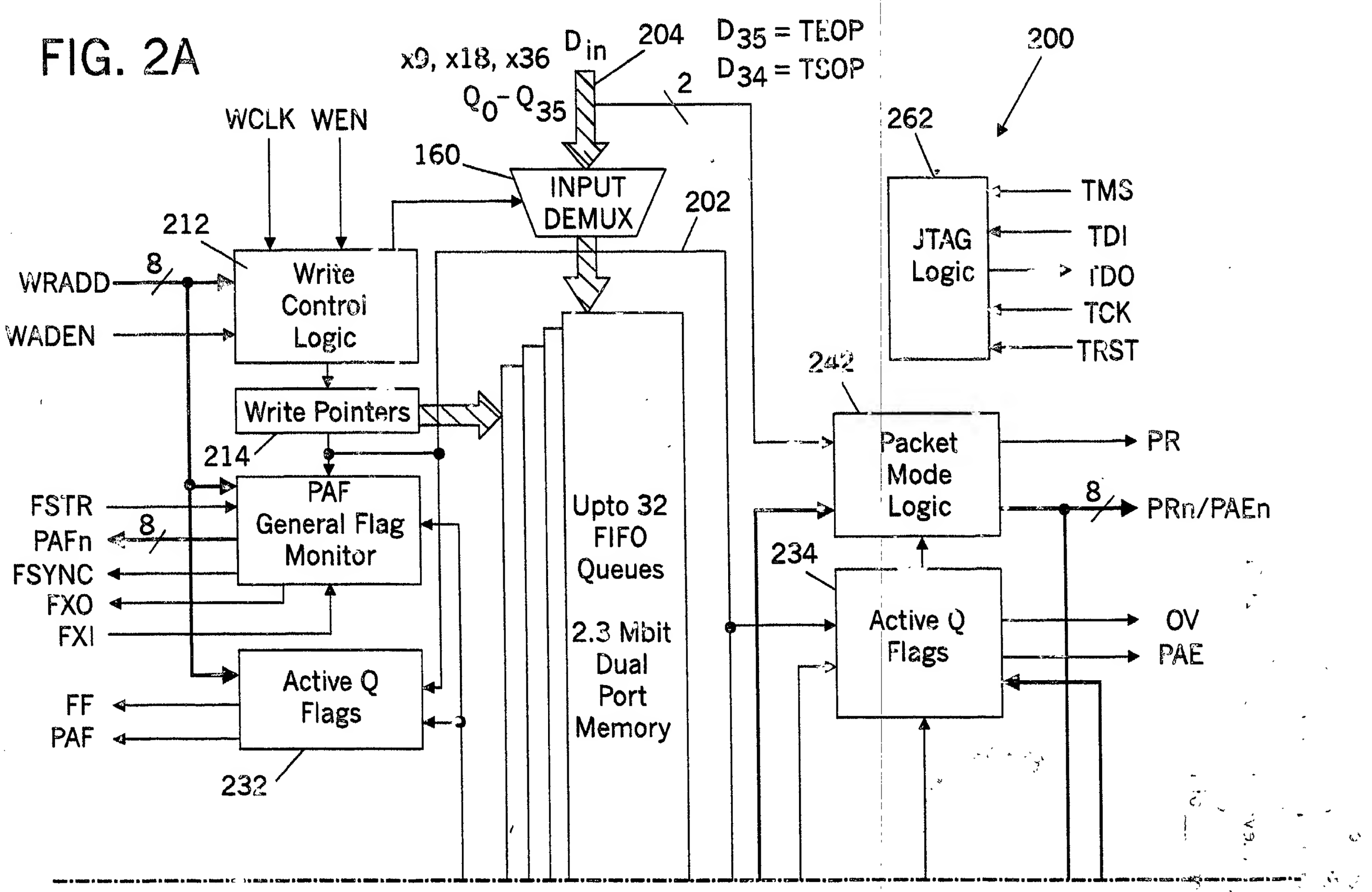

100
110
120
150a
WRITE
CONTROL
150c
READ CONTROL
WADEN
FSTR
WRADD
8
WEN
WCLK
RADEN
ESTR
RDADD
8
REN
RCLK
DE
Q0
Q1
Q2
Qmax
130
160
170
Din
x36
DATA IN
Qout
x36
DATA OUT
140
OV
PR
PAE
PAEn
8PRn
FF
PAF
PAFn
8
150b
WRITE
FLAGS
150d
READ FLAGS

FIG. 2A


x9, x18, x36
D_{in}
204
D_{35} = TEOP
D_{34} = TSOP
Q_0-Q_{35}
2
200
262
WCLK
WEN
160
INPUT DEMUX
202
212
JTAG Logic
TMS
TDI
TDO
TCK
TRST
WRADD
8
WADEN
Write Control Logic
242
Write Pointers
214
Packet Mode Logic
PR
8
PRn/PAEn
FSTR
8
PAFn
FSYNC
FXO
FXI
PAF General Flag Monitor
Upto 32 FIFO Queues
234
Active Q Flags
OV
PAE
2.3 Mbit Dual Port Memory
FF
PAF
Active Q Flags
232

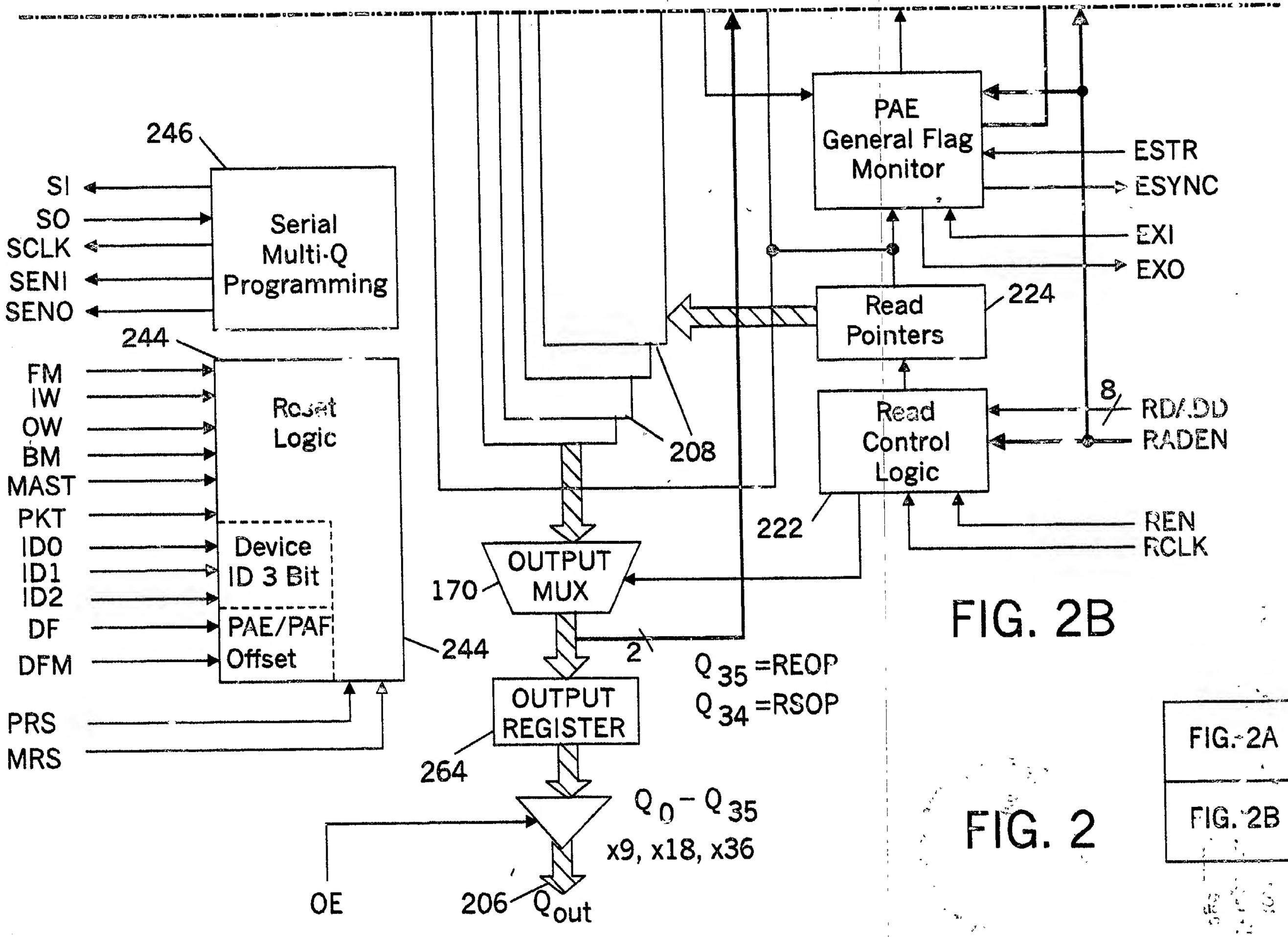

246
SI
SO
SCLK
SENI
SENO
Serial
Multi-Q
Programming
244
FM
IW
OW
BM
MAST
PKT
ID0
ID1
ID2
DF
DFM
Reset
Logic
Device
ID 3 Bit
PAE/PAF
Offset
PRS
MRS
244
208
PAE
General Flag
Monitor
ESTR
ESYNC
EXI
EXO
Read
Pointers
224
Read
Control
Logic
8
RDADD
RADEN
222
REN
RCLK
OUTPUT
MUX
170
2
Q_{35} =REOP
Q_{34} =RSOP
OUTPUT
REGISTER
264
$Q_0 - Q_{35}$
x9, x18, x36
OE
206
Q_{out}

FIG. 2B

FIG. 2

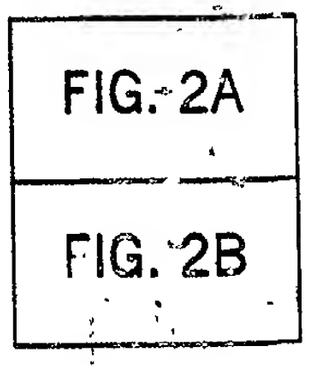


FIG. 2A
FIG. 2B

FIG. 3

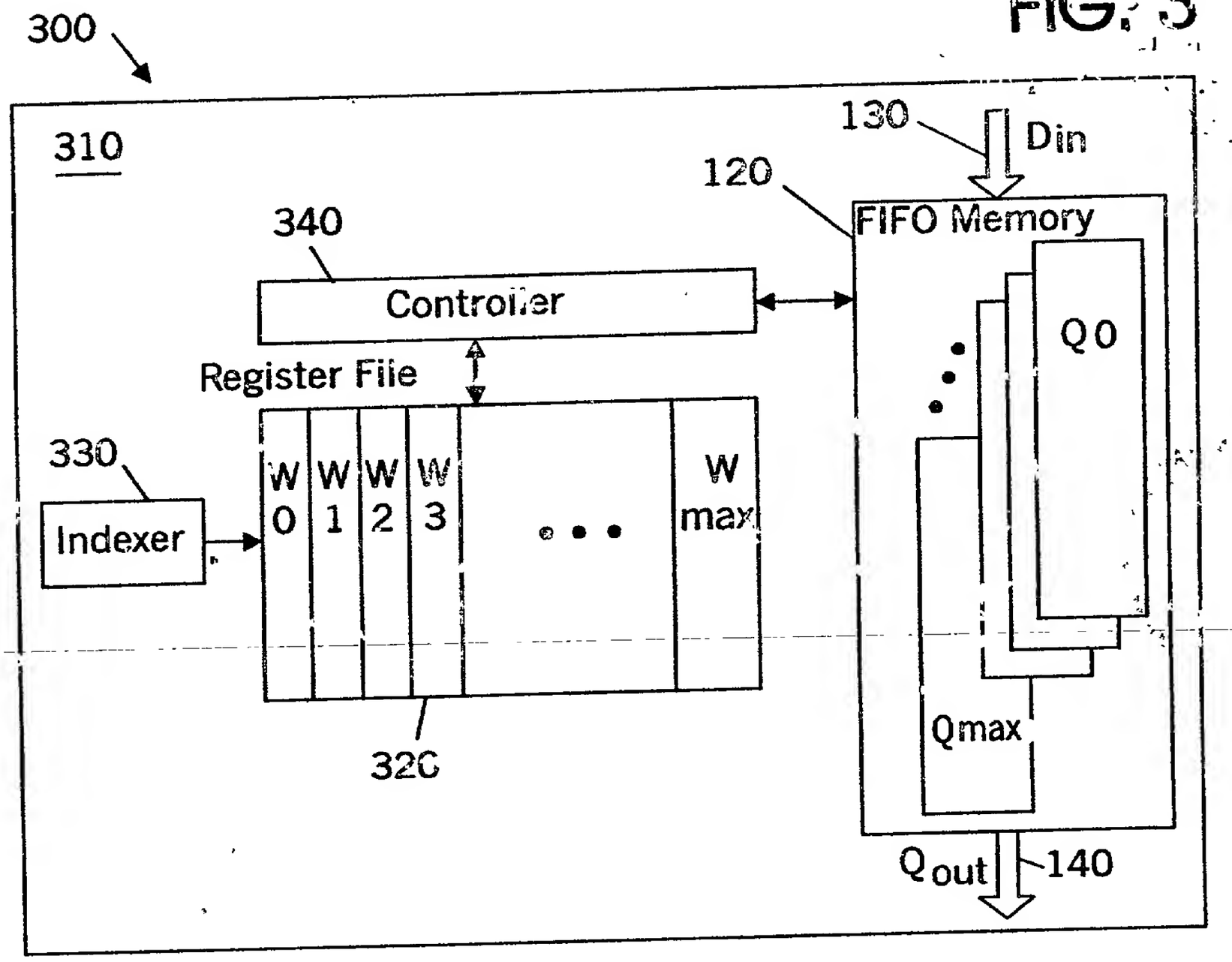

300
310
130
Din
120
FIFO Memory
340
Controller
Register File
Q0
330
Indexer
W 0
W 1
W 2
W 3
W max
Qmax
320
Qout
140

FIG. 4

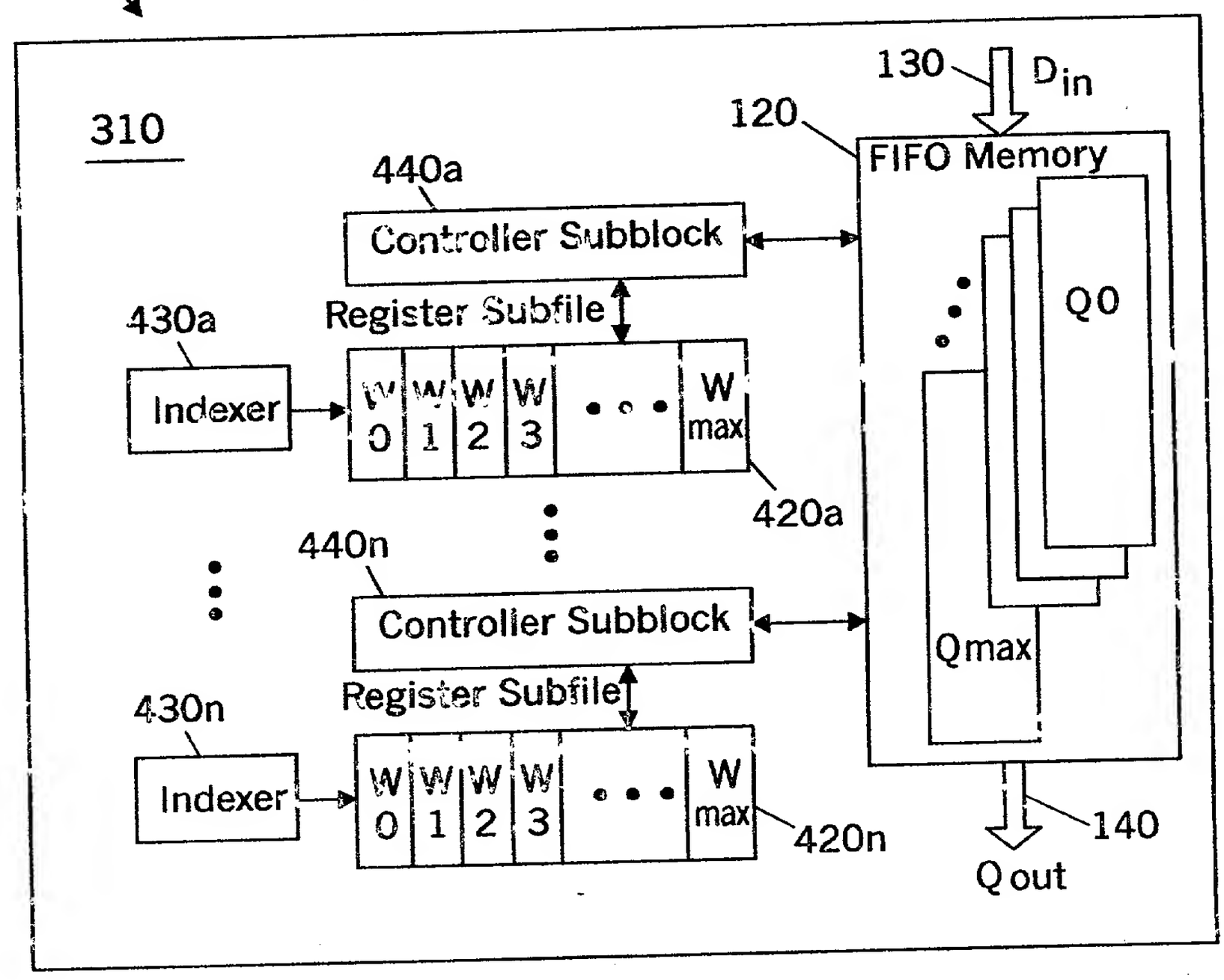
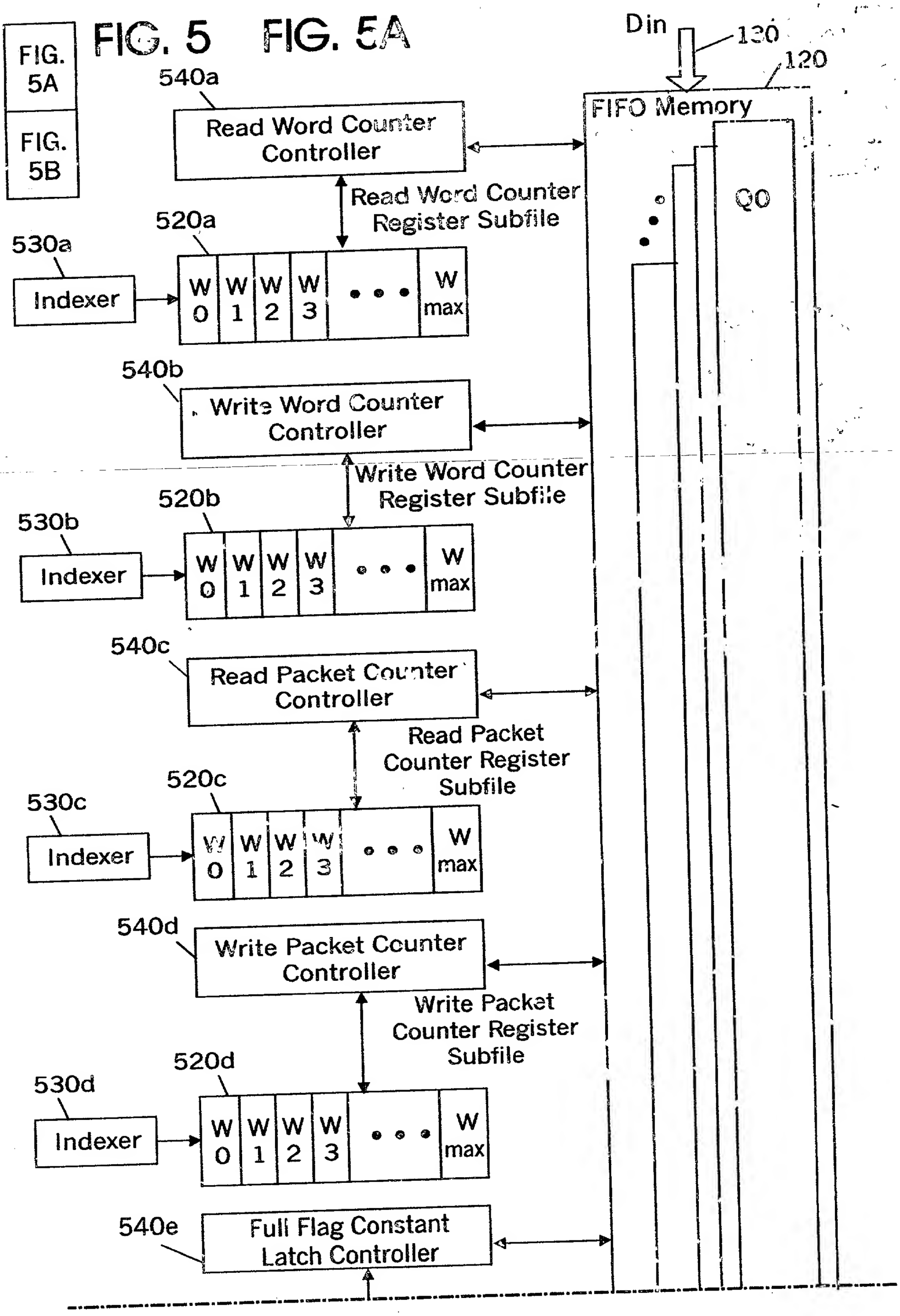

400
310
130
Din
120
FIFO Memory
440a
Controller Subblock
Register Subfile
Q0
430a
Indexer
W 0
W 1
W 2
W 3
W max
420a
440n
Controller Subblock
Register Subfile
Qmax
430n
Indexer
420n
140
Qout

FIG. 5 FIG. 5A

FIG. 5A
FIG. 5B



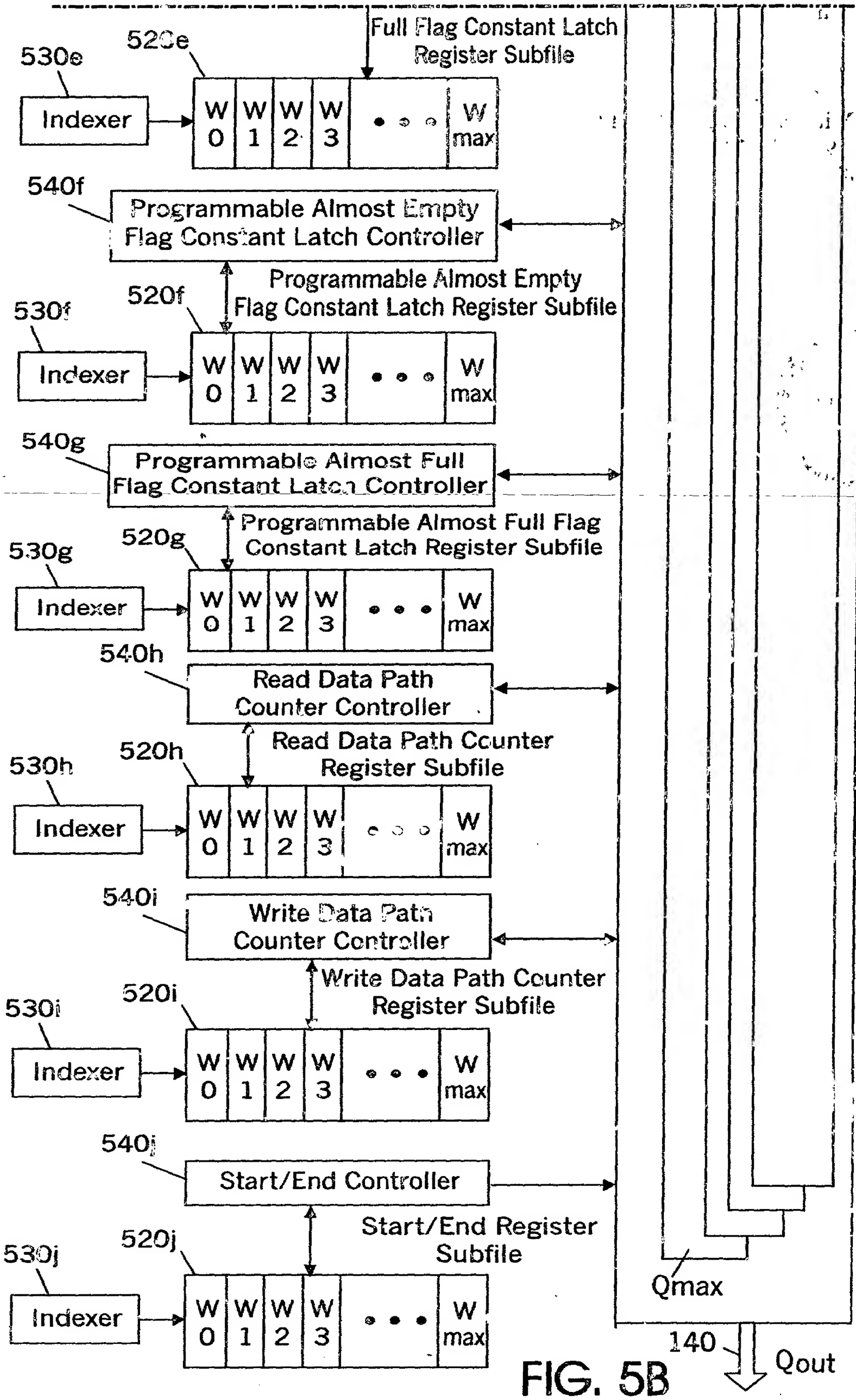

Full Flag Constant Latch Register Subfile
520e
530e
Indexer
W 0
W 1
W 2
W 3
W max
540f
Programmable Almost Empty Flag Constant Latch Controller
Programmable Almost Empty Flag Constant Latch Register Subfile
520f
530f
Indexer
540g
Programmable Almost Full Flag Constant Latch Controller
Programmable Almost Full Flag Constant Latch Register Subfile
520g
530g
Indexer
540h
Read Data Path Counter Controller
Read Data Path Counter Register Subfile
520h
530h
Indexer
540i
Write Data Path Counter Controller
Write Data Path Counter Register Subfile
520i
530i
Indexer
540j
Start/End Controller
Start/End Register Subfile
520j
530j
Indexer
Qmax
140
Qout

FIG. 5B

20070"662hh60

FIG. 6

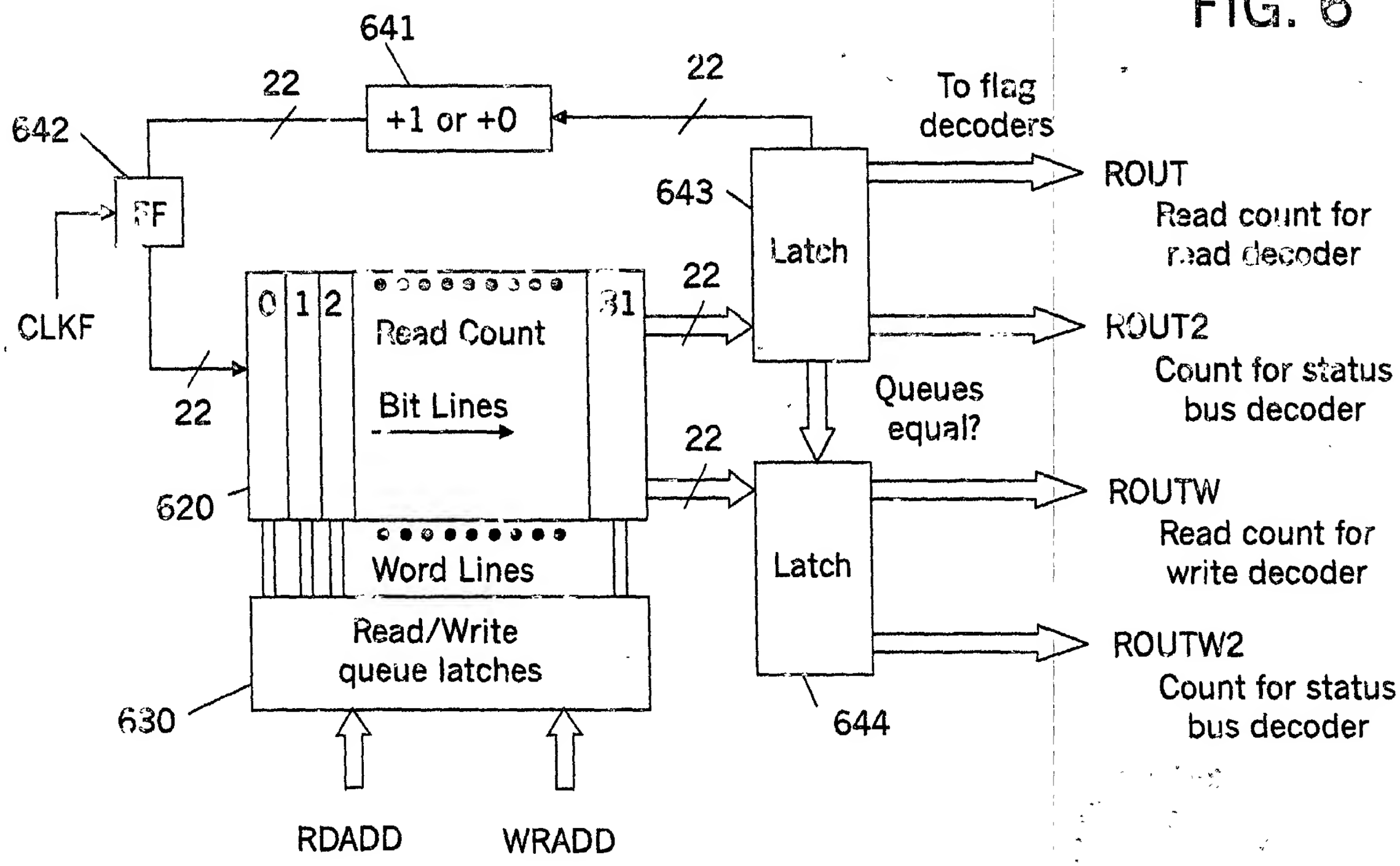


FIG. 7

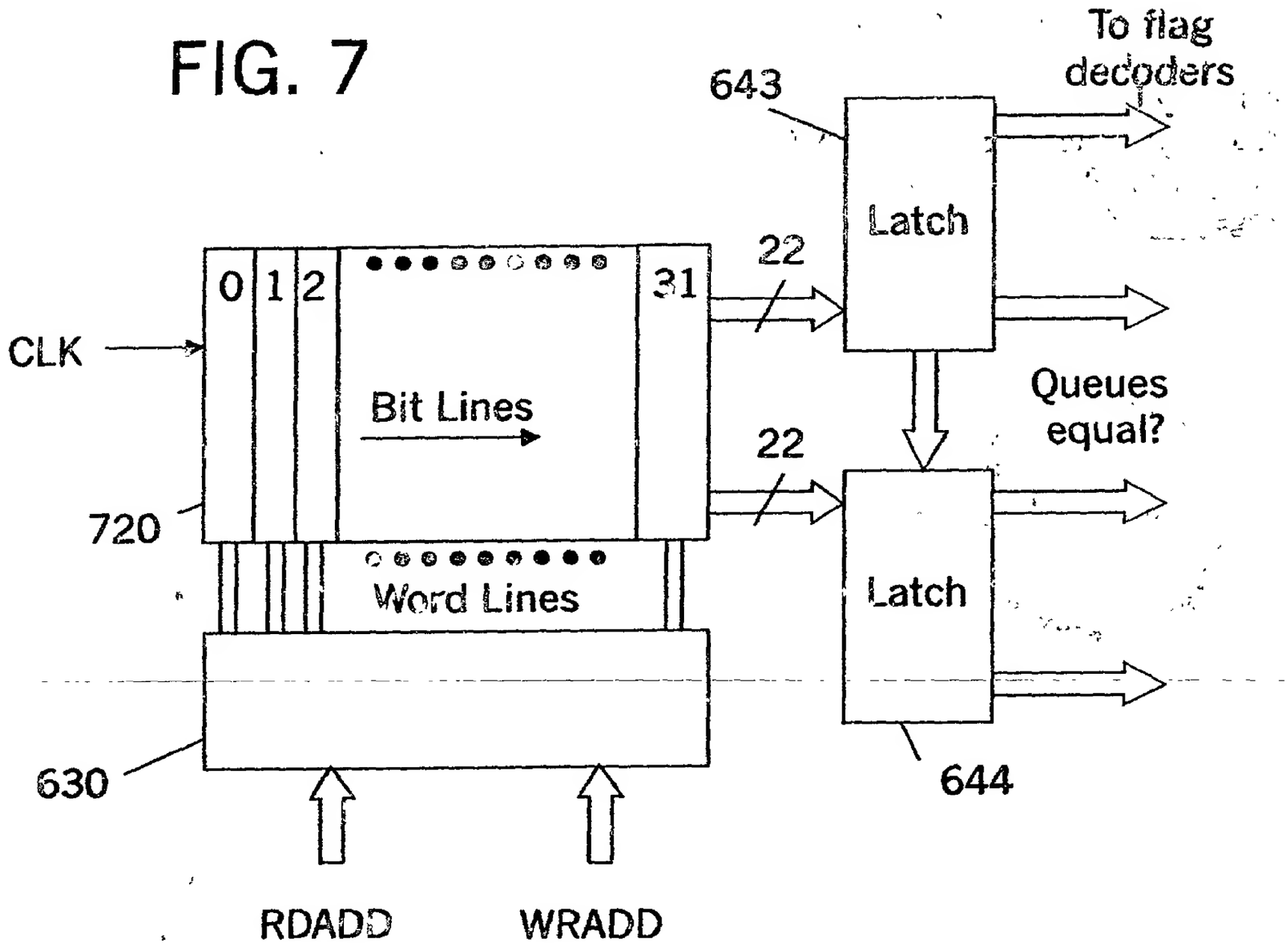

To flag decoders
643
Latch
22
0
1
2
31
CLK
Bit Lines
Queues equal?
22
720
Word Lines
Latch
630
644
RDADD
WRADD

FIG. 14

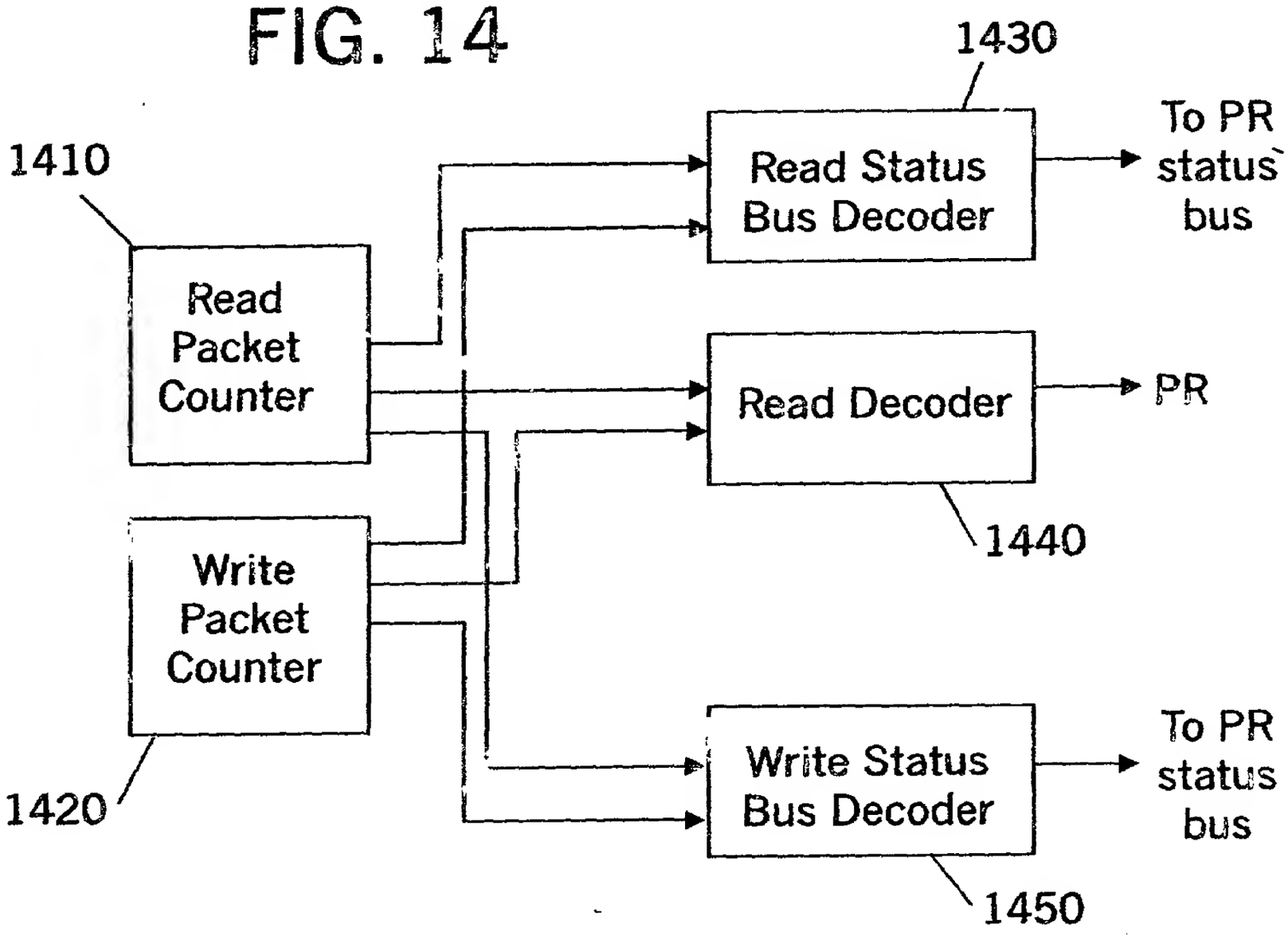

1430
To PR status bus
1410
Read Status Bus Decoder
Read Packet Counter
Read Decoder
PR
1440
Write Packet Counter
Write Status Bus Decoder
To PR status bus
1420
1450

FIG. 8

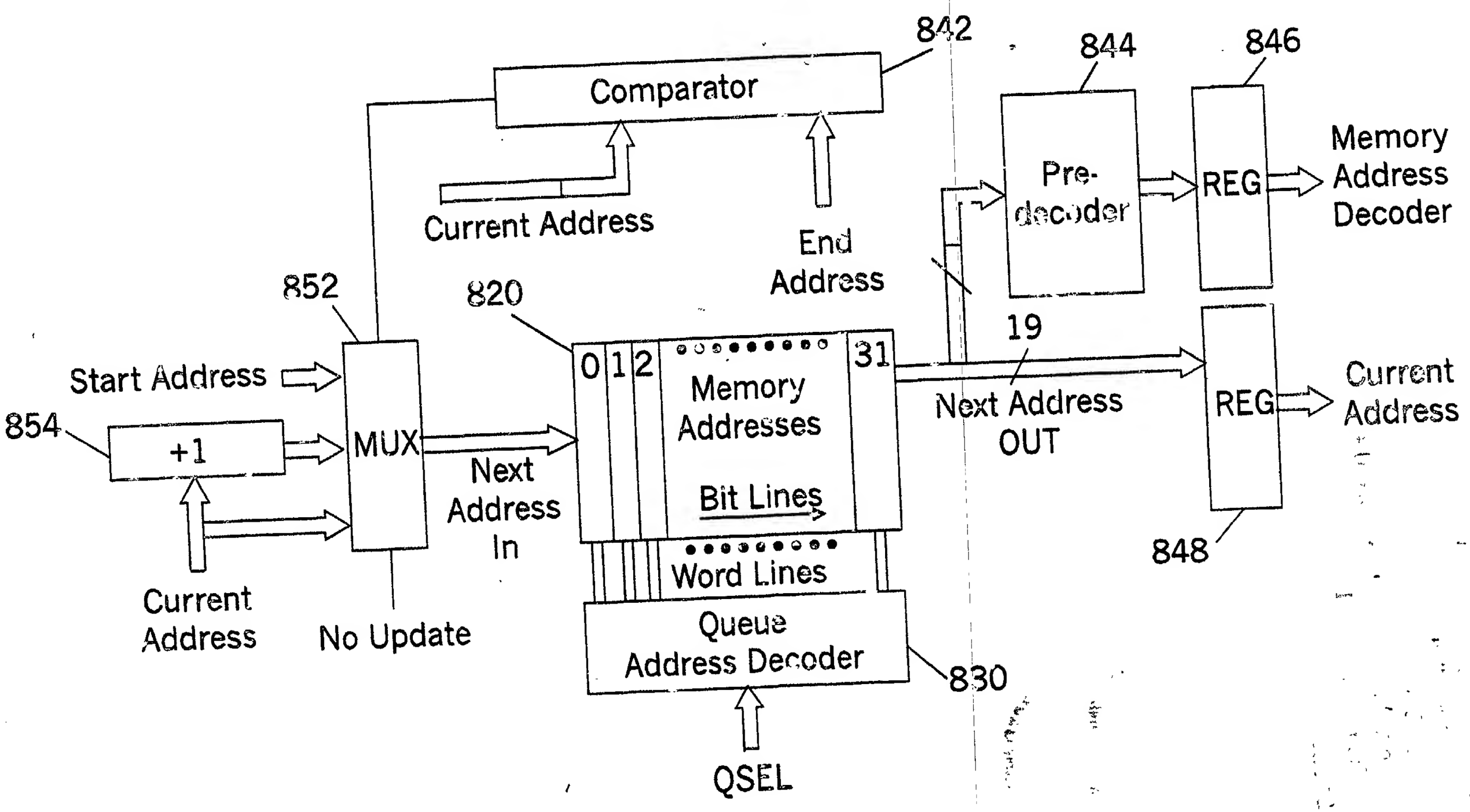

842
Comparator
Current Address
End Address
844
Pre-decoder
846
REG
Memory Address Decoder
852
820
19
Start Address
854
+1
MUX
Next Address In
0 1 2
Memory Addresses
31
Bit Lines
Word Lines
Next Address OUT
REG
Current Address
848
Current Address
No Update
Queue Address Decoder
830
QSEL

FIG. 9

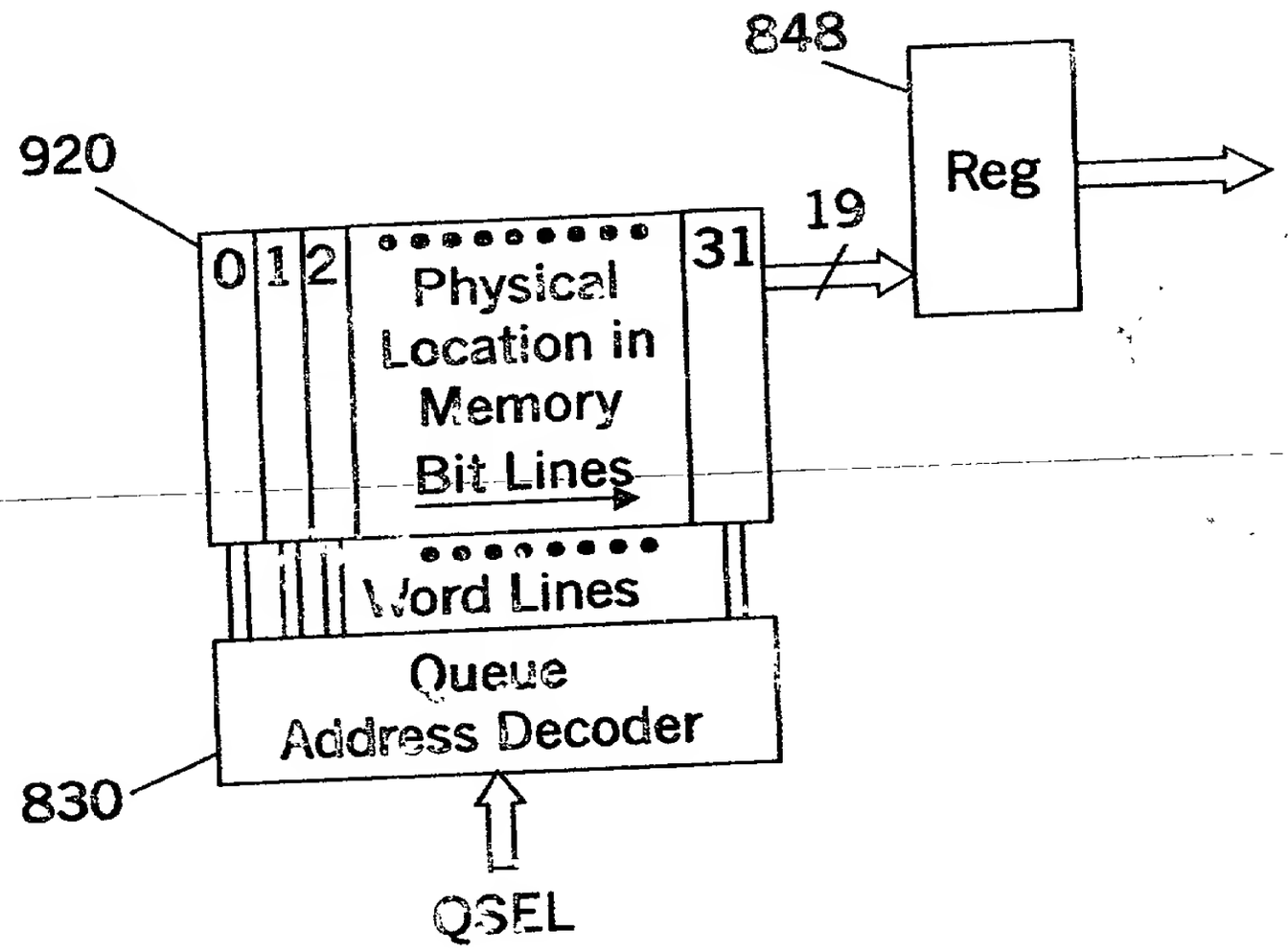

848
Reg
920
19
0
1
2
31
Physical
Location in
Memory
Bit Lines
Word Lines
Queue
Address Decoder
830
QSEL

FIG. 13

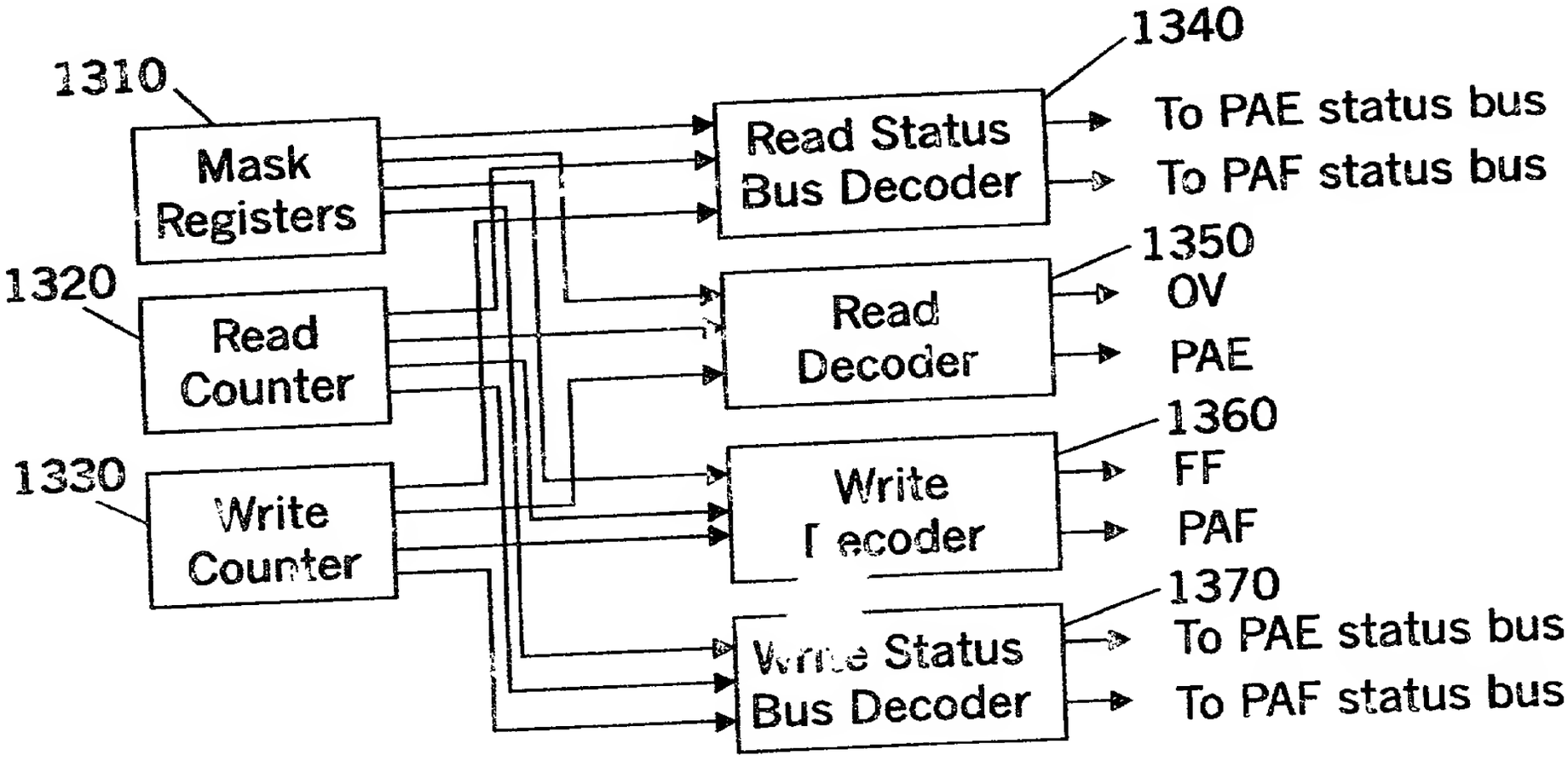

1310
Mask
Registers
1320
Read
Counter
1330
Write
Counter
1340
Read Status
Bus Decoder
To PAE status bus
To PAF status bus
1350
Read
Decoder
OV
PAE
1360
Write
Decoder
FF
PAF
1370
Write Status
Bus Decoder
To PAE status bus
To PAF status bus

FIG. 10

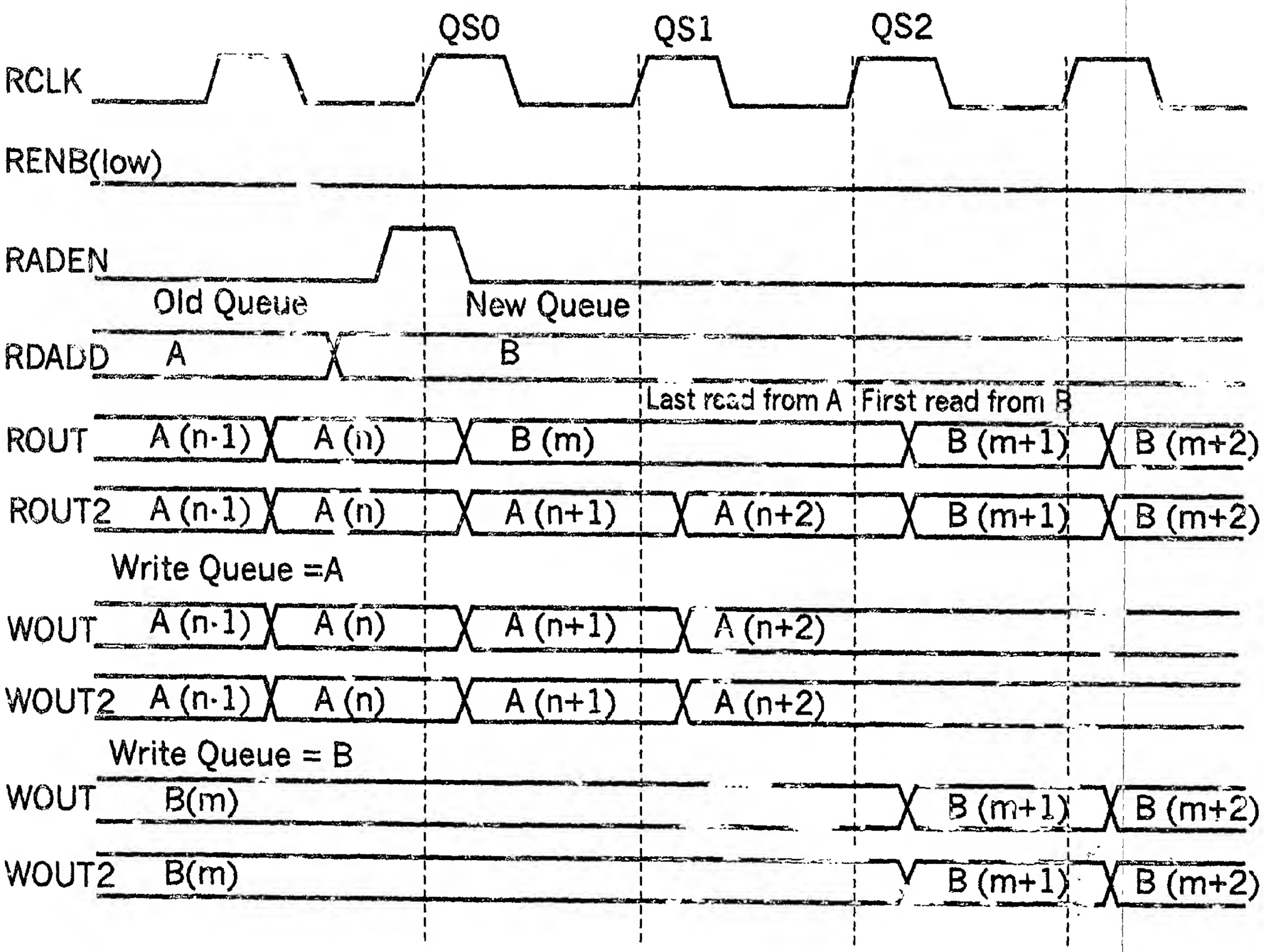
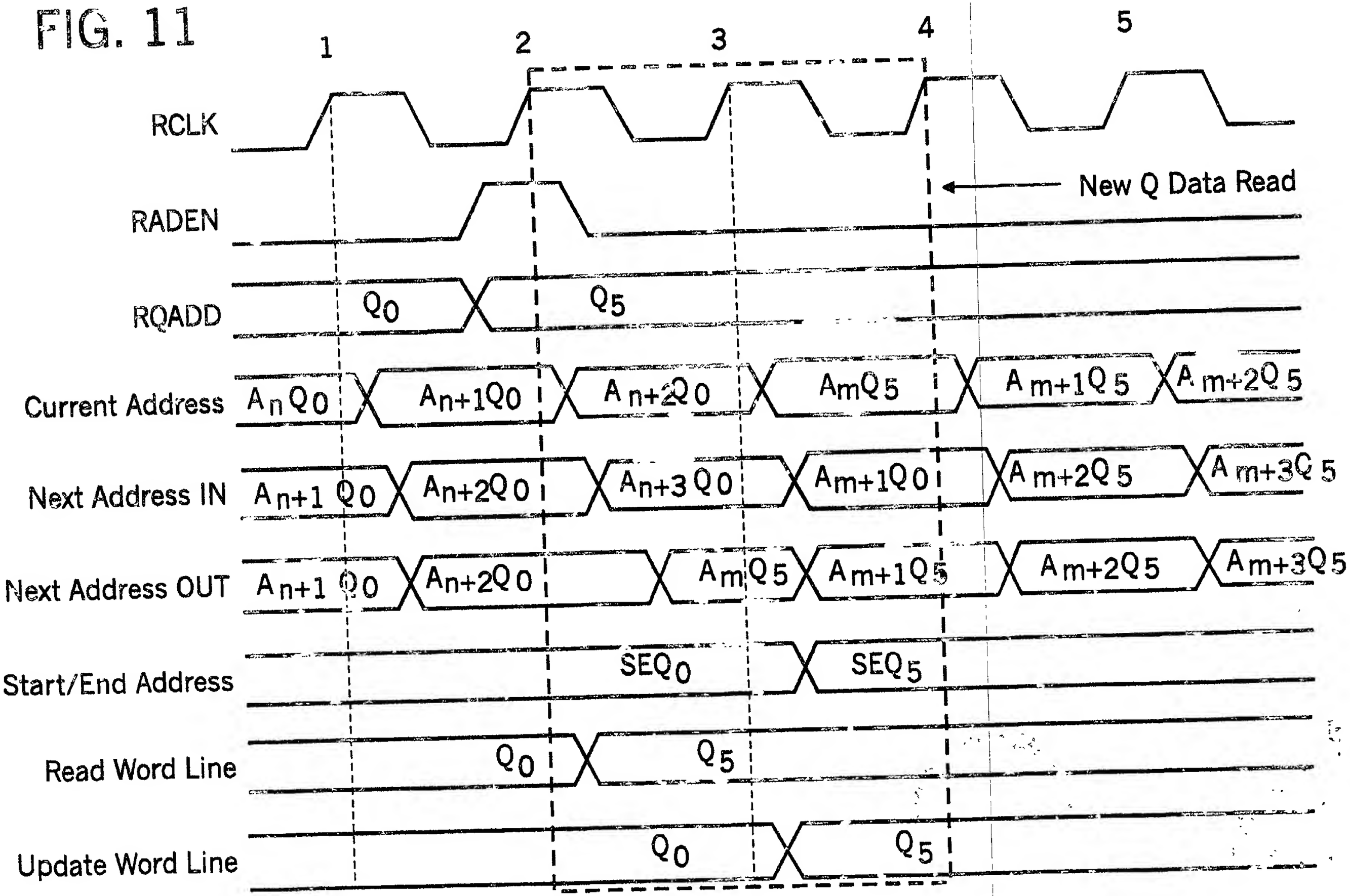

QS0
QS1
QS2
RCLK
RENB(low)
RADEN
Old Queue
New Queue
RDADD
A
B
Last read from A
First read from B
ROUT
A (n-1)
A (n)
B (m)
B (m+1)
B (m+2)
ROUT2
A (n-1)
A (n)
A (n+1)
A (n+2)
B (m+1)
B (m+2)
Write Queue =A
WOUT
A (n-1)
A (n)
A (n+1)
A (n+2)
WOUT2
A (n-1)
A (n)
A (n+1)
A (n+2)
Write Queue = B
WOUT
B(m)
B (m+1)
B (m+2)
WOUT2
B(m)
B (m+1)
B (m+2)

FIG. 11


1
2
3
4
5
RCLK
New Q Data Read
RADEN
RQADD
Q0
Q5
Current Address
An Q0
An+1Q0
An+2Q0
AmQ5
Am+1Q5
Am+2Q5
Next Address IN
An+1 Q0
An+2Q0
An+3Q0
Am+1Q0
Am+2Q5
Am+3Q5
Next Address OUT
An+1 Q0
An+2Q0
AmQ5
Am+1Q5
Am+2Q5
Am+3Q5
Start/End Address
SEQ0
SEQ5
Read Word Line
Q0
Q5
Update Word Line
Q0
Q5

2080T0" 6624hh660

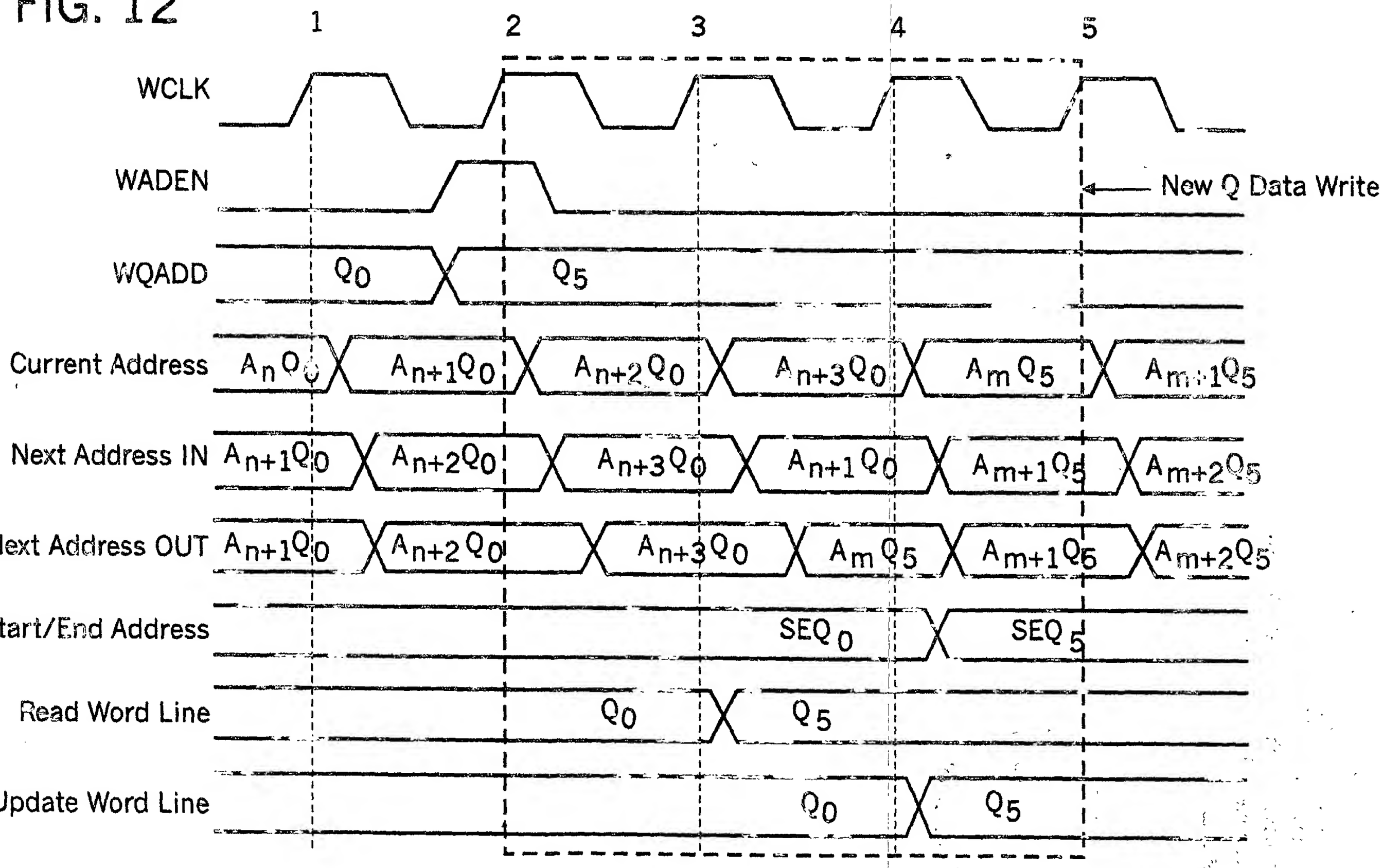



FIG. 12